Exhibit A

[redacted]

FORM PTO-1449 (modified)
To: U.S. Department of Commerce
Patent and Trademark Office

--REPLACEMENT--

INFORMATION DISCLOSURE STATEMENT FORM 1449

Page 1 of 1

Atty. Dkt. No.	043326-000-0021	Client Ref.

Inventor(s): **Jayesh R. BHAKTA et al.**

Patent No.: **7,619,912**

Date of Issue: **November 17, 2009**

Examiner: **SOFOCLEOUS, Alexander** | Group Art Unit: **2824**

U.S. PATENT DOCUMENTS

Examiner's Initials*		Document Number	Date MM/YYYY	Name (Family Name of First Inventor)	Class	Sub Class	Filing Date (if appropriate)
whc		2006/0117152	06-01-2006	AMIDI ET AL.	711	154	
↓		6,209,074	03-27-2001	DELL ET AL.	711	170	

FOREIGN PATENT DOCUMENTS

		Document Number	Date (dd/mm/yy)	Country	Applicant Name	English Abstract		Translation available	

OTHER (Including in this order Author, Title, Periodical Name, Date, Pertinent Pages, etc.)

whc		Murdocca, Miles J., Heuring, Vincent P.; Principles of Computer Architecture, Prentice Hall, Inc., Upper Saddle River, NJ, 2000; pp.243-252.
↓		"Quad Band Memory (QBMA™): DDR200/266/333 devices producing DDR400/533/667" (the "QBMA Reference"), published by the QBMA Alliance, Platform Conference, San Jose, California, January 23-24, 2002.
↓		JEDEC Standard No. 21-C, PC2100 and PC1600 DDR SDRAM Registered DIMM Design Specification, Revision 1.3, Release 11b, January 2002.

Examiner: [signature] Date Considered: 8/23/2010

*EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.

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Summary of Rejections

4. The following list is the summary of rejections in this Office action.

Ground 1: Obviousness over QBMA and JEDEC 21C (Proposed by Requester 1)

Proposed rejection of claim 1-17, 19, 21, and 23-51 is **not adopted**.

Ground 2: Obviousness over QBMA and Dell 2 (Proposed by Requester 1)

Proposed rejection of claim 1-17, 19, 21, and 23-51 is **not adopted**.

Ground 3: Anticipation by Amidi (Proposed by Requesters 1 and 2)

Rejection of claims 1-7, 9-11, 14-15, 18-21, 23-25, 28-34, 36-37, 40-43, 46, and 51, proposed by Requester 1, is **not adopted**.

Rejection of claims 1, 3-4, 6-11, 15, 18-22, 24-25, 27-29, 31-34, 36-39, and 41-45, and 50, proposed by Requester 2, is **not adopted**.

Ground 4: Obviousness over Amidi (Proposed by Requester 1)

Proposed rejection of claims 1-21, 23-25, 27-34, 36-43, 45-48, 50, and 51 is **not adopted**.

Proposed rejection of new claims 52-55, 57-59, 64-89, 92-108, and 112-118 is **not adopted**.

Ground 5: Obviousness over Amidi and Dell 2 (Proposed by Requester 1)

Proposed rejection of claims 1-51 is **not adopted**.

Ground 6: Obviousness over Amidi and JEDEC (Proposed by Requesters 1 and 2)

Rejection of claims 1, 3-4, 6, 8, 10, 11, 15, 18-20, 22, 24-25, 27-29, 31, 32, 34, 36-39, 41-43, 45, and 50, proposed by Requester 2 is **adopted**.

Rejection of claims 7, 9, 21, 33, and 44, proposed by Requester 2, is **not adopted**.

The Examiner rejects claims 12-14, 40, and 46-49.

Rejection of new claims 61-63, 90-91, and 109-111, proposed by Requester 1 is **adopted**.

Rejection of new claims 56 and 60, proposed by Requester 1, is **not adopted**.

Rejection of new claims 52, 61-65, 67-71, 75, 77-91, 94, 96, 98, 100, and 102-118, proposed by Requester 2, is **adopted**.

Rejection of new claims 53-60, 66, 72-74, 92-93, 95, 97, 99, and 101, proposed by Requester 2, is **not adopted**.

Ground 7: Obviousness over Murdocca and Dell 2 (Proposed by Requester 1)

Proposed rejection of claims 1-11, 14, 15, 19, 21, 23-25, 28-34, 36, 39-42 is **not adopted**.

Ground 8: Anticipation by Dell 1 (Proposed by Requester 2)

Proposed rejection of claims 1, 3-4, 6-9, 15, 18-22, 24-25, 27-29, 31-33, 36-39, 41-45, and 50 is **not adopted**.

Ground 9: Obviousness over Dell 1 and JEDEC standards (Proposed by Requester 2)

Proposed rejection of claims 1, 3-4, 6, 8, 15, 18-20, 22, 24-25, 27-29, 31, 32, 36-39, 41-43, 45, and 50 is **adopted**.

Proposed rejection of claims 7, 9, 21, 33, and 44 is **not adopted**.

Ground 10: Anticipation by Wong (Proposed by Requester 2)

Proposed rejection of claims 1, 3-4, 6-9, 15, 18-22, 24-25, 27-29, 31-33, 36-39, 41-45, and 50 is **not adopted**.

Ground 11: Obviousness over Wong and JEDEC standards (Proposed by Requester 2)

Proposed rejection of claims 1, 3-4, 6, 8, 15, 18-20, 22, 24-25, 27-29, 31, 32, 36-39, 41-43, 45, and 50 is **adopted**.

Proposed rejection of claims 7, 9, 21, 33, and 44 is **not adopted**.

Ground 12: Obviousness over Micron and Connelly (Proposed by Requester 3)

Proposed rejection of claims 1, 3-4, 6-8, 10, 11, 15, 18-20, 22, 24-25, 27-29, 31-33, 36-39, 41-45, and 50 is **adopted**.

Proposed rejection of claims 9 and 21 is **not adopted**.

The Examiner rejects claims 26 and 35.

Proposed rejection of new claims 64-65, 94, 96, 98, 102, 107, and 112-113 is **adopted**.

Proposed rejection of new claims 52-63, 66-93, 95, 97, 99-101, 103-106, 108-111, and 114-118 is **not adopted**.

Ground 13: Obviousness over Micron and Amidi (Proposed by Requester 3)

Proposed rejection of claims 1, 3-4, 6-8, 10, 11, 15, 18-20, 22, 24-25, 27-29, 31-34, 36-39, 41-45, and 50 is **adopted.**

Proposed rejection of claims 9 and 21 is **not adopted**.

The Examiner rejects claim 26.

Proposed rejection of new claims 52, 53, 61-65, 67-71, 75-91, 94, 96, 98, 100, and 102-118 is **adopted**.

Proposed rejection of new claims 54-60, 66, 72-74, 92-93, 95, 97, 99, and 101 is **not adopted**.

Ground 14: Lack of written description support (Proposed by Requesters 1 and 3)

Rejection of claims 57-60, 68, 76, 79, 84, and 89-91, proposed by Requester 1 is **not adopted**.

Rejection of claims 92-101 and 115-118, proposed by Requester 3, is **adopted**.

Ground 15: Lack of enablement (Proposed by Requester 3)

Proposed rejection of claims 115-118 is **adopted**.

Proposed rejection of claims 68-70, 76, 78, 82, 88, 94, 96, 98, 100, is **not adopted**.

Ground 16: Indefiniteness (Proposed by Requesters 1 and 3)

Rejection of claim 76, proposed by Requester 1, is **not adopted**.

Rejection of claims 116-118, proposed by Requester 3, is **adopted**.

Rejection of claims 64, 65, 68, 76, 87, 94, 95, 97, 99, 101, 102-108, 112-115, proposed by Requester 3, is **not adopted.**

Ground 17: Obviousness over Amidi, JEDEC, and Vogt (Proposed by Requester 2)

Proposed rejection of claim 76 is **adopted**.

Ground 18: Obviousness over Micron, Connelly and Dell 2 (Proposed by Requester 3)

Proposed rejection of claims 1, 15, 28, and 39 is **adopted**.

Ground 19: Obviousness over Micron, Amidi, and Dell 2 (Proposed by Requester 3)

Proposed rejection of claim 21 is **not adopted**.

Discussion of Rejections

Ground 1

Docket No.: 635162800300
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Inter Partes Reexamination of:
Jayesh BHAKTA et al.

Examiner: Woo H. CHOI

Control Nos.: 95/000,578; 95/000,579; 95/001,339

Art Unit: 3992

Filed: October 20, 2010; October 21, 2010; June 8, 2010

Conf. No.: 5035

For: MEMORY MODULE DECODER

RESPONSE/AMENDMENT

MS Inter Partes Reexam
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

INTRODUCTORY COMMENTS

In response to the Office Action dated October 14, 2011, for which a response was due on December 14, 2011, and for which a one-month extension of time to extend the time for response from December 14, 2011 to January 17, 2012 (the first business day after January 14, 2012) was requested and granted, please consider the following.

There are no amendments to the specification or drawings.

Claim amendments begin on page 1 and continue to page 45.

Status of all claims is provided at page 46.

Remarks/Arguments begin on page 47.

An explanation of support for the new claims added with this Amendment begins on page 59.

A certificate of service is provided at page 63.

la-1154468

first side and the memory devices of the fourth set are spaced from the memory devices of the third set in a direction along the second side.

12. (Original) The memory module of claim 1, wherein the plurality of DDR memory devices comprises a plurality of DDR2 memory devices arranged in a first rank, a second rank, a third rank, and a fourth rank, the first rank and the second rank on a first side of the printed circuit board, the third rank and the fourth rank on a second side of the printed circuit board, the second side different from the first side.

13. (Original) The memory module of claim 12, wherein the first rank is spaced from the second rank and the third rank is spaced from the fourth rank.

14. (Original) The memory module of claim 1, wherein the set of input control signals corresponds to a first memory density, and the set of output control signals corresponds to a second memory density, the second memory density greater than the first memory density.

15. (Amended) A memory module connectable to a computer system, the memory module comprising:

a printed circuit board;

a plurality of double-data-rate (DDR) memory devices coupled to the printed circuit board, the plurality of DDR memory devices having a first number of DDR memory devices arranged in a first number of ranks;

a circuit coupled to the printed circuit board, the circuit comprising a logic element and a register, the logic element receiving a set of input signals from the computer system, the set of input signals comprising at least one row/column address signal, bank address signals, and at least one

chip-select signal, the set of input signals configured to control a second number of DDR memory devices arranged in a second number of ranks, the second number of DDR memory devices smaller than the first number of DDR memory devices and the second number of ranks less than the first number of ranks, the circuit generating a set of output signals in response to the set of input signals, the set of output signals configured to control the first number of DDR memory devices arranged in the first number of ranks, wherein the circuit further responds to a command signal and the set of input signals from the computer system by selecting one or two ranks of the first number of ranks and transmitting the command signal to at least one DDR memory device of the selected one or two ranks of the first number of ranks; and

a phase-lock loop device coupled to the printed circuit board, the phase-lock loop device operatively coupled to the plurality of DDR memory devices, the logic element, and the register,

wherein the logic element generates gated column access strobe (CAS) signals or chip-select signals of the output signals in response at least in part to a bank address signal of the set of input signals.

16. (Amended) [The memory module of claim 15] A memory module connectable to a computer system, the memory module comprising:

a printed circuit board;

a plurality of double-data-rate (DDR) memory devices coupled to the printed circuit board, the plurality of DDR memory devices having a first number of DDR memory devices arranged in a first number of ranks;

a circuit coupled to the printed circuit board, the circuit comprising a logic element and a register, the logic element receiving a set of input signals from the computer system, the set of input signals comprising at least one row/column address signal, bank address signals, and at least one chip-select signal, the set of input signals configured to control a second number of DDR memory devices arranged in a second number of ranks, the second number of DDR memory devices smaller than the first number of DDR memory devices and the second number of ranks less than the first number of ranks, the circuit generating a set of output signals in response to the set of input signals, the set of output signals configured to control the first number of DDR memory devices arranged in the first number of ranks, wherein the circuit further responds to a command signal and the set of input signals from the computer system by selecting one or two ranks of the first number of ranks and transmitting the command signal to at least one DDR memory device of the selected one or two ranks of the first number of ranks; and

a phase-lock loop device coupled to the printed circuit board, the phase-lock loop device operatively coupled to the plurality of DDR memory devices, the logic element, and the register,

wherein the command signal is transmitted to only one DDR memory device at a time.

17. (Original) The memory module of claim 16, wherein the command signal comprises a read command signal.

18. (Original) The memory module of claim 15, wherein the command signal is transmitted to two ranks of the first number of ranks at a time.

19. (Original) The memory module of claim 18, wherein the command signal comprises a refresh command signal.

under § 102, (2) claims 1, 3, 4, 6, 10–20, 24, 25, 27–29, 31, 32, 34, 36–43, 45–48, 50, 52–54, 56, 58, 67–71, 75, 77–89, 92, 93, 120–126, 128–130, 132, 133, and 135 based on Amidi under § 103, (3) claims 56, 60–63, 90, 91, 109–111, 127, and 131 based on Amidi and JEDEC under § 103, (4) claims 16 and 17 based on Amidi and Dell 2, and (5) claims 58, 60, 68, 79, 84, 89–91, 128–131 under § 112, ¶ 1 as lacking written description support.

We reverse the Examiner's decision not to adopt the rejections of claims 1, 3, 4, 6, 8, 10–15, 18–20, 22, 24, 25, 27–29, 31, 32, 34–43, 45–50, 52–54, 56, 58, 60–63, 67–71, 75, 77–93, 109–111, and 120–136 based on (1) Amidi and Dell 2, (2) Micron and Amidi, or (3) Micron, Amidi, and Olarig (Grounds 5, 13, and 21), designating our reversal as new grounds of rejection under 37 C.F.R. § 41.77(b).

We do not reach the propriety of the remaining adopted or proposed rejections.

V. TIME PERIOD FOR RESPONSE

Pursuant to 37 C.F.R. § 41.77(a), the above-noted reversal constitutes a new ground of rejection. Section 41.77(b) provides that "[a] new ground of rejection . . . shall not be considered final for judicial review." That section also provides that Patent Owner, WITHIN ONE MONTH FROM THE DATE OF THE DECISION, must exercise one of the following two options with respect to the new grounds of rejection to avoid termination of the appeal proceeding as to the rejected claims:

> (1) *Reopen prosecution.* The owner may file a response requesting reopening of prosecution before the examiner. Such a response must be either an amendment of the claims so rejected or new evidence relating to the claims so rejected, or both.

> see MPEP § 2662. First requests for extensions of these time periods will be granted for sufficient cause, and for a reasonable time specified-usually one month. The reasons stated in the request will be evaluated, and the request will be favorably considered where there is a factual accounting of reasonably diligent behavior by all those responsible for preparing a response or comments within the statutory time period. Second or subsequent requests for extensions of time, or requests for more than one month, will be granted only in extraordinary situations.

ANALYSIS

Patent Owner's request for an extension of time has been considered fully. The Decision on appeal includes three new grounds of rejection for claims 1, 3, 4, 6, 8, 10-15, 18-20, 22, 24, 25, 27-29, 31, 32, 34-43, 45-50, 52-54, 56, 58, 60-63, 67-71, 75, 77-93, 109-111, and 120-136 based on (1) Amidi and Dell 2, (2) Micron and Amidi, or (3) Micron, Amidi, and Olarig (Grounds 5, 13, and 21) under 37 C.F.R. § 41.77(b). Decision 70–102.

In accordance with 37 C.F.R. § 41.77(g), the time period set forth in paragraph (b) of this section is subject to the extension of time provisions of § 1.956 of this title when the Patent Owner is responding under paragraph (b)(1) of this section. First requests for extensions of these time periods will be granted for sufficient cause, and for a reasonable time specified, i.e., usually one month. The reasons stated in the request will be evaluated, and the request will be favorably considered where there is a factual accounting of reasonably diligent behavior by all those responsible for preparing a response or comments within the statutory time period. Second or subsequent requests for extensions of time, or requests for more than one month, will be granted only in extraordinary situations.

I hereby certify that this paper is being transmitted via the Office electronic filing system in accordance with § 1.6(a)(4).

Dated: July 31, 2016 Signature: /Erwin B. Palines/ (Erwin B. Palines)

VIA EFS
Docket No.: 635162800300
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Inter Partes Reexamination of:
Jayesh BHAKTA et al.

Examiner: Behzad PEIKARI

Control Nos.: 95/001,339; 95/000,578; 95/000,579

Art Unit: 3992

Filed: June 8, 2010; October 20, 2010; October 21, 2010

Conf. No.: 5035; 8810; 3547

For: MEMORY MODULE DECODER

PATENT OWNER'S RESPONSE REQUESTING TO REOPEN PROSECUTION PURSUANT TO 37 C.F.R. § 41.77(b)(1)

MS *Inter Partes* Reexam
Central Reexamination Unit
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

Dear Sir:

In response to the Patent Trial and Appeal Board's Decision dated May 31, 2016 (the "Decision"), for which a response requesting to reopen prosecution pursuant to 37 C.F.R. § 41.77(b)(1) was due June 30, 2016, and for which a one-month request for extension of time was requested and granted to July 31, 2016, the Patent Owner respectfully submits this Response. Please consider the following:

There are no amendments to the specification or drawings.

Claim amendments begin on page 2 of this paper.

Status of all claims is provided at page 46.

Remarks/Arguments begin on page 47, and a certificate of service is provided at page 58.

la-1322110

CLAIM AMENDMENTS

Please **cancel** claims 25, 42, 53, 68, 79, 84, 89, 92, 93, 121, 124, and 128-130.

Please **enter** the following amendments.

1. (Twice amended) A memory module connectable to a computer system, the memory module comprising:

a printed circuit board;

a plurality of double-data-rate (DDR) memory devices mounted to the printed circuit board, the plurality of DDR memory devices having a first number of DDR memory devices arranged in a first number of ranks;

a circuit mounted to the printed circuit board, the circuit comprising a logic element and a register, the logic element receiving a set of input control signals from the computer system, the set of input control signals comprising at least one row/column address signal, bank address signals, and at least one chip-select signal, the set of input control signals corresponding to a second number of DDR memory devices arranged in a second number of ranks, the second number of DDR memory devices smaller than the first number of DDR memory devices and the second number of ranks less than the first number of ranks, the circuit generating a set of output control signals in response to the set of input control signals, the set of output control signals corresponding to the first number of DDR memory devices arranged in the first number of ranks, wherein the circuit further responds to a first command signal and the set of input control signals from the computer system by generating and transmitting a second command signal and the set of output control signals to the plurality of memory devices, the first command signal and the set of input control

signals corresponding to the second number of ranks and the second command signal and the set of output control signals corresponding to the first number of ranks; and

a phase-lock loop device mounted to the printed circuit board, the phase-lock loop device operatively coupled to the plurality of DDR memory devices, the logic element, and the register,

wherein, in response to signals received from the computer system, the phase-lock loop (PLL) device transmits a PLL clock signal to the plurality of DDR memory devices, the logic element, and the register,

wherein, the register (i) receives, from the computer system, and (ii) buffers, in response to the PLL clock signal, a plurality of row/column address signals and the bank address signals, and (iii) transmits the buffered plurality of row/column address signals and the buffered bank address signals to the plurality of DDR memory devices, wherein the at least one row/column address signal received by the logic element comprises at least one row address signal received by the logic element, and wherein the plurality of row/column address signals received by the register are separate from the at least one row address signal received by the logic element, and

wherein the logic element generates gated column access strobe (CAS) signals or chip-select signals of the output control signals in response at least in part to (i) the at least one row address signal, (ii) the bank address signals, and (iii) the at least one chip-select signal of the set of input control signals and (iv) the PLL clock signal.

2. (Amended) [The memory module of claim 1] A memory module connectable to a computer system, the memory module comprising:

a printed circuit board;

a plurality of double-data-rate (DDR) memory devices mounted to the printed circuit board, the plurality of DDR memory devices having a first number of DDR memory devices arranged in a first number of ranks;

a circuit mounted to the printed circuit board, the circuit comprising a logic element and a register, the logic element receiving a set of input control signals from the computer system, the set of input control signals comprising at least one row/column address signal, bank address signals, and at least one chip-select signal, the set of input control signals corresponding to a second number of DDR memory devices arranged in a second number of ranks, the second number of DDR memory devices smaller than the first number of DDR memory devices and the second number of ranks less than the first number of ranks, the circuit generating a set of output control signals in response to the set of input control signals, the set of output control signals corresponding to the first number of DDR memory devices arranged in the first number of ranks, wherein the circuit further responds to a first command signal and the set of input control signals from the computer system by generating and transmitting a second command signal and the set of output control signals to the plurality of memory devices, the first command signal and the set of input control signals corresponding to the second number of ranks and the second command signal and the set of output control signals corresponding to the first number of ranks; and

a phase-lock loop device mounted to the printed circuit board, the phase-lock loop device operatively coupled to the plurality of DDR memory devices, the logic element, and the register,

wherein the circuit is configured to store an input control signal of the set of input control signals during a row access procedure and to transmit the stored input control signal as an output control signal of the set of output control signals during a column access procedure.

3. (Original) The memory module of claim 1, wherein the set of input control signals comprises a first number of chip-select signals and wherein the set of output control signals comprises a second number of chip-select signals greater than the first number of chip-select signals.

4. (Original) The memory module of claim 3, wherein the first number of chip-select signals is two and the second number of chip-select signals is four.

5. (Amended) [The memory module of claim 1] A memory module connectable to a computer system, the memory module comprising:

a printed circuit board;

a plurality of double-data-rate (DDR) memory devices mounted to the printed circuit board, the plurality of DDR memory devices having a first number of DDR memory devices arranged in a first number of ranks;

a circuit mounted to the printed circuit board, the circuit comprising a logic element and a register, the logic element receiving a set of input control signals from the computer system, the set of input control signals comprising at least one row/column address signal, bank address signals, and at least one chip-select signal, the set of input control signals corresponding to a second number of DDR memory devices arranged in a second number of ranks, the second number of DDR memory devices smaller than the first number of DDR memory devices and the second number of

ranks less than the first number of ranks, the circuit generating a set of output control signals in response to the set of input control signals, the set of output control signals corresponding to the first number of DDR memory devices arranged in the first number of ranks, wherein the circuit further responds to a first command signal and the set of input control signals from the computer system by generating and transmitting a second command signal and the set of output control signals to the plurality of memory devices, the first command signal and the set of input control signals corresponding to the second number of ranks and the second command signal and the set of output control signals corresponding to the first number of ranks; and

a phase-lock loop device mounted to the printed circuit board, the phase-lock loop device operatively coupled to the plurality of DDR memory devices, the logic element, and the register,

wherein the circuit receives and buffers a plurality of row/column address signals of the input control signals during a row access procedure and sends the buffered plurality of row/column address signals to the plurality of DDR memory devices during a subsequent column access procedure.

6. (Original) The memory module of claim 1, wherein the logic element comprises an application-specific integrated circuit, a field-programmable gate array, a custom-designed semiconductor device, or a complex programmable-logic device.

7. (Amended) [The memory module of claim 1] A memory module connectable to a computer system, the memory module comprising:

a printed circuit board;

a plurality of double-data-rate (DDR) memory devices mounted to the printed circuit board, the plurality of DDR memory devices having a first number of DDR memory devices arranged in a first number of ranks;

a circuit mounted to the printed circuit board, the circuit comprising a logic element and a register, the logic element receiving a set of input control signals from the computer system, the set of input control signals comprising at least one row/column address signal, bank address signals, and at least one chip-select signal, the set of input control signals corresponding to a second number of DDR memory devices arranged in a second number of ranks, the second number of DDR memory devices smaller than the first number of DDR memory devices and the second number of ranks less than the first number of ranks, the circuit generating a set of output control signals in response to the set of input control signals, the set of output control signals corresponding to the first number of DDR memory devices arranged in the first number of ranks, wherein the circuit further responds to a first command signal and the set of input control signals from the computer system by generating and transmitting a second command signal and the set of output control signals to the plurality of memory devices, the first command signal and the set of input control signals corresponding to the second number of ranks and the second command signal and the set of output control signals corresponding to the first number of ranks; and

a phase-lock loop device mounted to the printed circuit board, the phase-lock loop device operatively coupled to the plurality of DDR memory devices, the logic element, and the register,

wherein the bank address signals of the set of input control signals are received by both the logic element and the register.

8. (Original) The memory module of claim 1, wherein two or more of the phase-lock loop device, the register, and the logic element are portions of a single component.

9. (Amended) [The memory module of claim 1] A memory module connectable to a computer system, the memory module comprising:

a printed circuit board;

a plurality of double-data-rate (DDR) memory devices mounted to the printed circuit board, the plurality of DDR memory devices having a first number of DDR memory devices arranged in a first number of ranks;

a circuit mounted to the printed circuit board, the circuit comprising a logic element and a register, the logic element receiving a set of input control signals from the computer system, the set of input control signals comprising at least one row/column address signal, bank address signals, and at least one chip-select signal, the set of input control signals corresponding to a second number of DDR memory devices arranged in a second number of ranks, the second number of DDR memory devices smaller than the first number of DDR memory devices and the second number of ranks less than the first number of ranks, the circuit generating a set of output control signals in response to the set of input control signals, the set of output control signals corresponding to the first number of DDR memory devices arranged in the first number of ranks, wherein the circuit further responds to a first command signal and the set of input control signals from the computer system by generating and transmitting a second command signal and the set of output control signals to the plurality of memory devices, the first command signal and the set of input control

signals corresponding to the second number of ranks and the second command signal and the set of output control signals corresponding to the first number of ranks; and

a phase-lock loop device mounted to the printed circuit board, the phase-lock loop device operatively coupled to the plurality of DDR memory devices, the logic element, and the register,

wherein the register comprises a plurality of register devices.

10. (Original) The memory module of claim 1, wherein the plurality of DDR memory devices is arranged as a first set of DDR memory devices on a first side of the printed circuit board, a second set of DDR memory devices on the first side of the printed circuit board, a third set of DDR memory devices on a second side of the printed circuit board, and a fourth set of DDR memory devices on the second side of the printed circuit board, the DDR memory devices of the second set spaced from the DDR memory devices of the first set, the DDR memory devices of the fourth set spaced from the DDR memory devices of the third set.

11. (Original) The memory module of claim 10, wherein the DDR memory devices of the second set are spaced from the DDR memory devices of the first set in a direction along the first side and the memory devices of the fourth set are spaced from the memory devices of the third set in a direction along the second side.

12. (Original) The memory module of claim 1, wherein the plurality of DDR memory devices comprises a plurality of DDR2 memory devices arranged in a first rank, a second rank, a third rank, and a fourth rank, the first rank and the second rank on a first side of the printed circuit board, the third rank and the fourth rank on a second side of the printed circuit board, the second side different from the first side.

13. (Original) The memory module of claim 12, wherein the first rank is spaced from the second rank and the third rank is spaced from the fourth rank.

14. (Original) The memory module of claim 1, wherein the set of input control signals corresponds to a first memory density, and the set of output control signals corresponds to a second memory density, the second memory density greater than the first memory density.

15. (Twice amended) A memory module connectable to a computer system, the memory module comprising:

a printed circuit board;

a plurality of double-data-rate (DDR) memory devices coupled to the printed circuit board, the plurality of DDR memory devices having a first number of DDR memory devices arranged in a first number of ranks;

a circuit coupled to the printed circuit board, the circuit comprising a logic element and a register, the logic element receiving a set of input signals from the computer system, the set of input signals comprising at least one row/column address signal, bank address signals, and at least one chip-select signal, the set of input signals configured to control a second number of DDR memory devices arranged in a second number of ranks, the second number of DDR memory devices smaller than the first number of DDR memory devices and the second number of ranks less than the first number of ranks, the circuit generating a set of output signals in response to the set of input signals, the set of output signals configured to control the first number of DDR memory devices arranged in the first number of ranks, wherein the circuit further responds to a command signal and the set of input signals from the computer system by selecting one or two ranks of the first number of ranks

and transmitting the command signal to at least one DDR memory device of the selected one or two ranks of the first number of ranks; and

a phase-lock loop device coupled to the printed circuit board, the phase-lock loop device operatively coupled to the plurality of DDR memory devices, the logic element, and the register,

wherein, in response to signals received from the computer system, the phase-lock loop (PLL) device transmits a PLL clock signal to the plurality of DDR memory devices, the logic element, and the register,

wherein, the register (i) receives, from the computer system, and (ii) buffers, in response to the PLL clock signal, a plurality of row/column address signals and the bank address signals, and (iii) transmits the buffered plurality of row/column address signals and the buffered bank address signals to the at least one DDR memory device of the selected one or two ranks of the first number of ranks, wherein the at least one row/column address signal received by the logic element comprises at least one row address signal received by the logic element, and wherein the plurality of row/column address signals received by the register are separate from the at least one row address signal received by the logic element, and

wherein the logic element generates gated column access strobe (CAS) signals or chip-select signals of the output signals in response at least in part to (i) the at least one row address signal, (ii) the bank address signals and (iii) the at least one chip-select signal of the set of input signals and (iv) the PLL clock signal.

16. (Amended) [The memory module of claim 15] A memory module connectable to a computer system, the memory module comprising:

a printed circuit board;

a plurality of double-data-rate (DDR) memory devices coupled to the printed circuit board, the plurality of DDR memory devices having a first number of DDR memory devices arranged in a first number of ranks;

a circuit coupled to the printed circuit board, the circuit comprising a logic element and a register, the logic element receiving a set of input signals from the computer system, the set of input signals comprising at least one row/column address signal, bank address signals, and at least one chip-select signal, the set of input signals configured to control a second number of DDR memory devices arranged in a second number of ranks, the second number of DDR memory devices smaller than the first number of DDR memory devices and the second number of ranks less than the first number of ranks, the circuit generating a set of output signals in response to the set of input signals, the set of output signals configured to control the first number of DDR memory devices arranged in the first number of ranks, wherein the circuit further responds to a command signal and the set of input signals from the computer system by selecting one or two ranks of the first number of ranks and transmitting the command signal to at least one DDR memory device of the selected one or two ranks of the first number of ranks; and

a phase-lock loop device coupled to the printed circuit board, the phase-lock loop device operatively coupled to the plurality of DDR memory devices, the logic element, and the register,

wherein the command signal is transmitted to only one DDR memory device at a time.

17. (Original) The memory module of claim 16, wherein the command signal comprises a read command signal.

REMARKS

I. Introduction

On May 31, 2016, the Patent Trial and Appeal Board (the "Board") issued a Decision affirming the Examiner in part. In the Decision, the Board issued a number of new grounds of rejection. (Decision at 102.) The Patent Owner responds by respectfully requesting to reopen prosecution before the Examiner pursuant to 37 C.F.R. § 41.77(b)(1). This Response includes both claim amendments and evidence – the accompanying Second Supplemental Declaration of Dr. Carl Sechen pursuant to 37 C.F.R. § 1.132 – to overcome the new grounds of rejection.

With respect to the claim amendments, the Patent Owner has made the following principle amendments to overcome the new grounds of rejection:

- Phase Lock Loop (PLL) Device
- Register
- Logic Element

The amendments are detailed in Section II. The Patent Owner respectfully submits that the claims, as amended, overcome the new grounds of rejection as detailed in Sections III-VI and in the accompanying Second Supplemental Sechen Declaration.

II. Claim Amendments and Discussion of Support

The '912 Patent has four original independent claims: claims 1, 15, 28, and 39. Previously, claims 52, 57, 67, 77, 82, and 87 were added independent claims. The amendments to the claims are discussed below with a discussion of support pursuant to 37 C.F.R. §§ 1.530(e) and 1.941. It is also noted that Section I of the Second Supplemental Sechen Declaration ("Second Supp. Sechen Decl.") provides a detailed analysis of the support for the claim amendments.

A. Phase Lock Loop (PLL) Device

Claim 1 is amended to recite (exemplary support citations in curly braces):

> a phase-lock loop device mounted to the printed circuit board, the phase-lock loop device operatively coupled to the plurality of DDR memory devices, the logic element, and the register,
>
> wherein, in response to signals received from the computer system {5:28}, the phase-lock loop (PLL) device {50 in Figs. 1A, 1B} transmits a PLL clock signal {5:29} to the plurality of DDR memory devices, the logic element, and the register {5:29-31}[.]

Claims 15, 28, 39, 52, 67, 77, 82 and 87 have identical or nearly identical recitations. *See also* Second Supp. Sechen Decl. at ¶ 10.

B. Register

Next, the Patent Owner has amended claim 1 to recite (exemplary support citations in curly braces):

> a register…
>
> wherein, the register {60 in Figs. 1A, 1B} (i) receives, from the computer system {5:31}, and (ii) buffers, in response to the PLL clock signal {Figs. 1A, 1B; 5:31}, a plurality of row/column address signals {7:43-45} and the bank address signals {7:50-51}, and (iii) transmits the buffered plurality of row/column address signals and the buffered bank address signals to the plurality of DDR memory devices {30 in Figs. 1A, 1B; 5:34-36}, wherein the at least one row/column address signal received by the logic element comprises at least one row address signal received by the logic element, and wherein the plurality of row/column address signals received by the register {A_0-A_n in Figs. 1A, 1B} are separate from the at least one row address signal received by the logic element {A_{n+1} in Figs. 1A, 1B}[.]

Claims 15, 28, 39, 52, 67, 77, 82 and 87 have identical or nearly identical recitations. *See also* Second Suppl. Sechen Decl. at ¶ 11.

C. Logic Element

Additionally, claim 1 is amended to recite (exemplary support citations in curly braces):

> the logic element receiving a set of input control signals from the computer system, the set of input control signals comprising at least one row/column address signal, bank address signals, and at least one chip-select signal, …
>
> wherein the logic element generates gated column access strobe (CAS) signals or chip-select signals {Figs. 1A, 1B, 3A, 3B; 17:28-19:521 22:50-63; 23:6-25} of the output control signals in response {6:55-63} at least in part to (i) the at least one row address signal {A_{n+1} in Figs. 1A, 1B; A13 in Figs. 3A, 3B; 7:46-53}, (ii) [a] the bank address signals {B_0-B_m in Figs. 1A, 1B; BA_0, BA_1 in Figs. 3A, 3B; 7:46-53}, and (iii) the at least one chip-select signal {CS_0, CS_1 in Fig. 1A; CS_0 in Fig. 1B; 7:46-53} of the set of input control signals and (iv) the PLL clock signal {Figs. 1A, 1B; 5:29-30; "clk_in" in 17:28-19:52}.

Claims 15, 28, 39, 52, 67, 77, 82 and 87 have identical or nearly identical recitations. *See also* Second Suppl. Sechen Decl. at ¶ 12.

D. Other Amendments

A number of other amendments were made for conformity.

The dependency of claim 43 has been changed to claim 39 in view of the cancellation of claim 42.

The dependency of new claim 54 has been changed to new claim 52 in view of the cancellation of new claim 53. The recitation of "wherein the transmission of the buffered bank address signals by the register is timed to the clock signals received from the phase-lock loop device, and the generation of the first number of chip-select signals by the logic element is timed to the clock signals received from the phase-lock loop device" previously in new claim 54 has been deleted in view of the amendment to new claim 52.

In new claim 123, the recitation "the logic element is responsive at least in part to a row address bit of the at least one row/column address signal, the bank address signals, and the at least one chip-select signal by generating" has been replaced by "the chip-select signals generated by the logic element are" in view of the amendment to claim 1.

The dependency of new claim 125 has been changed to new claim 123 in view of the cancellation of new claim 124. The phrase "the row address bit" has been changed to "the at least one row address signal" and the recitation "wherein the transmission of the buffered bank address signals by the register is timed to the clock signals received from the phase-lock loop device, and the generation of the first number of chip-select signals by the logic element is timed to the clock signals received from the phase-lock loop device" has been deleted in view of the amendment to claim 1.

The dependency of new claim 131 has been changed to claim 1 in view of the cancellation of new claims 128-130.

The dependency of new claim 134 has been changed to claim 15 in view of the cancellation of claim 25.

The term "the bank address signals" has been deleted from claims 134-136 in view of the amendments to claims 15, 28 and 39.

III. Claims 1, 3, 4, 6, 8, 10-15, 18-20, 22, 24, 25, 27-29, 31, 32, 34-43, 45-50, 120-122, and 132-136 Are Patentable Over Amidi In View Of Dell 2 (Ground 5)

Claims 1, 3, 4, 6, 8, 10-15, 18-20, 22, 24, 25, 27-29 , 31, 32, 34-43, 45-50, 120-122 and 132-136 have been rejected by the Board as obvious over Amidi in view of Dell 2. These amendments distinguish the claims from the combination of Amidi and Dell 2. *See* Second Supp. Sechen Decl. at Section II.

Dell 2 is cited for teaching or suggesting "a logic element receiving and using free signals, including a bank address signal", and Amidi is cited for its "suggestion to use other types of

memory devices." (Decision, 43.) The Decision then concludes that the combination of Amidi and Dell 2 teaches or suggests generating a chip-select, CAS, or rank selecting signal in response to a bank address signal. (Decision, 81.) To address the Board's rejection, Patent Owner narrowed the claim to include:

- "in response to signals received from the computer system, the phase-lock loop (PLL) device transmits a PLL clock signal to the plurality of DDR memory devices, the logic element, and the register"
- "the register (i) receives, from the computer system, and (ii) buffers, in response to the PLL clock signal, a plurality of row/column address signals and the bank address signals, and (iii) transmits the buffered plurality of row/column address signals and the buffered bank address signals to the plurality of DDR memory devices, wherein the at least one row/column address signal received by the logic element comprises at least one row address signal received by the logic element, and wherein the plurality of row/column address signals received by the register are separate from the at least one row address signal received by the logic element"
- "the logic element generates gated column access strobe (CAS) signals or chip-select signals of the output control signals in response at least in part to (i) the at least one row address signal, (ii) the bank address signals, and (iii) the at least one chip-select signal of the set of input control signals and (iv) the PLL clock signal."

As described herein, the claim amendments highlight at least two differences between the '912 invention and the prior art.

First, the claim amendments now require: in response to signals received from the computer system, the phase-lock loop (PLL) device transmit a PLL clock to the plurality of DDR memory devices, the logic element, and the register. Amidi transmits a PLL clock signal to the register and memory, but not to the CPLD. Thus, Amidi does not disclose the PLL device transmitting the PLL clock to the *logic element*; the output of PLL 606 is neither directly nor indirectly transmitted to the

CPLD 604. *See* Second Supp. Sechen Decl. at ¶¶ 18-19. Additionally, a POSITA would not be motivated or inclined to transmit the PLL clock to CPLD 604. *Id.* at ¶ 20.

Second, the amended claims now also require that the logic element generates certain output control signals (e.g., gated column access strobe (CAS) signals or chip-select signals recited in claim 1) in response at least in part to (i) the at least one row address signal, (ii) the bank address signals, and (iii) the at least one chip-select signal of the set of input control signals and (iv) the PLL clock signal. Amidi's CPLD 604 never receives bank address signals and hence Amidi's control signals cannot be generated based on bank address signals. Instead, the control signals (rcs0a, rcs0b, rcs1a, rcs1b, rcs2a, rcs2b, rcs3a, and rcs3b) are based on the row address signals and chip-select signals. Thus, Amidi does not disclose the CPLD generating the gated CAS signals or chip-select signals in response to *the bank address signals*. Second Supp. Sechen Decl. at ¶¶ 21-22. Moreover, since the output of PLL 606 is neither directly nor indirectly transmitted to the CPLD 604, a POSITA would understand that the PLL clock does not control the operation of CPLD 604. Thus, Amidi is further deficient by failing to disclose the CPLD generating the gated CAS signals or chip-select signals in response to the *PLL clock signal*. *Id.* at ¶ 18-19.

Dell 2 does not cure the deficiencies of Amidi with respect to the amended claim. Dell 2 merely discloses a remapping or reassignment of a row address bit (A12) to be used as a bank address bit (BA1). Dell 2 does not disclose using bank address signals to generate a chip-select signal or a CAS signal. Second Supp. Sechen Decl. at ¶ 25.

Even taken in combination, Amidi and Dell 2, it would not be obvious to a POSITA to modify Amidi's system to provide the bank address signals to the CPLD device, and generate chip-select signals based on the bank address signals and a row address signal. As amended, the claims require that the *logic element receives* at least one row address signal and *bank address signals*, and require that *the register* (i) *receives*, from the computer system, and (ii) buffers, in response to the PLL clock signal, a plurality of row/column address signals and *the bank address signals*, and (iii) transmits the buffered plurality of row/column address signals and the buffered bank address signals to the plurality of DDR memory devices. The claims also require the plurality of row/column

address signals received by the register are separate from the at least one row address signal received by the logic element. In other words, in the configuration recited by the claims, the bank address signals are received by the logic element, the register and the plurality of memory devices. Under such circumstances, Amidi does not use bank address signals to generate control signals (and certainly not the bank address signals and the at least one row address signal). The claims, however, require generating CAS signals or chip-select signals based on a row address signal and bank address signals. Second Supp. Sechen Decl. at ¶¶ 23-24 and 26.

Based on the above, it would not be obvious to a POSITA to combine Amidi and Dell 2 to reach the claimed invention, as amended. For the sake of argument, however, even the proposed combination of Amidi and Dell 2 fails to disclose the claimed invention. Therefore, even in combination, Amidi in view of Dell 2 fails to disclose all of the claim recitations of the claims.

While claims 132-133 are patentable over Ground 5 based on amended claim 15 from which they depend, these claims are patentable for an additional reason. Specifically, claim 132 (and its dependent claim 133) recite that "the command signal is transmitted to only one DDR memory device at a time." Claim 16 (and its dependent claim 17) have a similar recitation, and the Board found that Amidi and Dell 2 were deficient as to this recitation. (Decision, 75-77, 82-83.) Based on that reasoning, claims 132 and 133 are similarly patentable over Ground 5. It is believed that the inclusion of these claims under Ground 5 has been in error.

IV. Claims 1, 3, 4, 6, 8, 10-15, 18-20, 22, 24, 25, 27-29, 31, 32, 36-39, 41-43, 45, 50, 52-54, 56, 58, 60-63, 67-71, 75, 77-93, 109-111, and 120-136 Are Patentable Over Micron In View Of Amidi (Ground 13)

Claims 1, 3, 4, 6, 8, 10, 11, 15, 18-20, 22, 24, 25, 27-29, 31, 32, 36-39, 41-43, 45, 50, 52-54, 56, 58, 60-63, 67-71, 75, 77-93, 109-111, and 120-136 have been rejected by the Board as obvious over Micron in view of Amidi.

The Decision relied on two different cases proposed by Requester 3 to reject the claims. The first case refers to a memory controller that generates one row address signal more than the actual

memory devices use (Decision, 94), and the second case refers to a memory controller that generates one bank address signal more than the actual memory devices use (Decision, 94-95.)

As discussed above, the claims, as amended, are directed to a logic element separately receiving a row address signal (i.e., similar to the first case). As claimed, the registers, and thereby the plurality of memory devices, use the bank address signals. Thus, the amended claims exclude the second case involving one more bank address signal than required by the actual memory devices. In other words, the rationale of the second case does not apply to the amended claims.

Instead, the claims require that the logic element receives at least one row address signal separate from the address signals received by the register, and as discussed above, Amidi does not suggest using a bank address signal for generating CAS signals or chip-select signals (or rank multiplication) when a row address signal is not used by the actual memory devices. Additionally, Amidi provides no recognition to use both the bank address signals and a row address signal for rank multiplication or the generation of chip-select signals or CAS signal signals. Second Supp. Sechen Decl. at ¶ 29.

The Decision rejects the claims under the first case based on what a POSITA "would have recognized regarding bank address signals, as well as other signals, in the context of memory modules." (Decision, 95.) The Decision concludes, based on Requester 3's expert, Dr. Kozyrakis, that a POSITA would have recognized to use bank address signals to generate chip-select signals. (*Id.*, 96.) Additionally, the Decision concludes that a POSITA, employing their background knowledge, would have known that additional signals are needed to generate the chip-select signals and would turn to bank address signals in order to multiply ranks. (*Id.*, 97.) But, Amidi already claims to provide rank multiplication without the use of bank address signals. Second Supp. Sechen Decl. at ¶ 30.

The conclusions of Requester 3's expert at best represent how an expert, not a POSITA, would understand Amidi's disclosure. There is no question that a POSITA would recognize the conventional use of bank address signals in Amidi, but there is no suggestion of using the bank

address signal for rank multiplication or the generation of chip-select signals or CAS signal signals. Amidi is representative evidence of what a POSITA would understand. No cited art suggests a recognition of the need for bank address signals for rank multiplication, or for generation of CAS signals or chip-select signals. Amidi was plainly not aware of any need – as the bank address signals are not used to generate the chip select signals. A POSITA reading Amidi would have recognized that Amidi claims to achieve rank multiplication without bank signals for generating chip-select signals and would not have recognized an unconventional use for the bank address signals. Second Supp. Sechen Decl. at ¶ 31.

Dr. Kozyrakis, an expert, says that bank address signals are necessary for proper generation of chip select signals, but a POSITA taking Amidi at face value would have understood otherwise. Amidi provides no recognition to use both the bank address signals and a row address signal for rank multiplication or the generation of chip-select signals or CAS signal signals. Second Supp. Sechen Decl. at ¶ 32.

Regardless of whether bank address signals are necessary for proper operation, this is a conclusion of fact and not an indication of what a POSITA would recognize. Amidi's complete omission of using bank address signals is formidable evidence that a POSITA looking at Amidi would not think bank address signals are necessary. Rather a POSITA would conclude that Amidi is operative without bank address signals for generating control signals. To suggest otherwise forces upon Amidi an operating principle that is not present. Namely the recognition that bank address signals are a necessary input for generating chip-select signals, when Amidi clearly does not. Second Supp. Sechen Decl. at ¶ 33.

Requester 3's expert asserts that "the nature of standard DDR commands motivates a person of ordinary skill in the art to use bank address signals to generate chip-select signals." (Decision, 96 (internal citations omitted).) While I agree that a POSITA is not an automaton and possesses common sense, understanding the nature of standard DDR commands is a skill level of an expert. A POSITA possesses far less creativity and skill than an expert, and in view of Amidi would not entertain the nature of standard DDR commands. A POSITA reading of Amidi would give some

deference to Amidi and understand that its principle of operation does not require bank address signals for generation of chip-select signals. Second Supp. Sechen Decl. at ¶ 34.

Ultimately, regardless of how necessary bank address signals are for generation of chip-select signals, Amidi was plainly unaware of this necessity. It is precisely recognition of this necessity and solution which underlie Netlist's discovery. Second Supp. Sechen Decl. at ¶ 35.

Based on the above, it would not be obvious to a POSITA to combine Micron and Amidi to reach the claimed invention, as amended. For the sake of argument, however, even the proposed combination of Micron and Amidi fails to disclose the claimed invention. Therefore, even in combination, Micron in view of Amidi fails to disclose all of the claim recitations in the claims.

While claims 132-133 are patentable over Ground 13 based on amended claim 15 from which they depend, these claims are patentable for an additional reason. Requester 3 never presented a proposed rejection for claims 132 and 133 under Ground 13 during the reexamination. *See* Requester 3's February 2012 Response, 23-25. It is believed that the inclusion of these claims under Ground 13 has been in error.

V. Claims 52-54, 56, 67-71, 77-79, 82-84, and 87-89 Are Patentable Over Amidi In View Of Dell 184 (Ground 20)

Claims 52-54, 56, 67-71, 77-79, 82-84, and 87-89 have been rejected by the Board as obvious over Amidi in view of Dell 184.

These amendments distinguish the claims from the combination of Amidi and Dell 184, as discussed above. *See also* Second Supp. Sechen Decl. Section IV.

VI. Claims 1, 3, 4, 6, 8, 10-15, 18-20, 22, 24, 25, 27-29, 31, 32, 34-43, 45-50, 52-54, 56, 58, 60-63, 67-71, 75, 77-93, 109-11, and 120-126 Are Patentable Over Micron In View Of Amidi, Further In View Of Olarig (Ground 21)

Claims 52-54, 67-71, 77-79, 82-84, and 87-89 have been rejected by the Board as obvious over Micron in view of Amidi and Olarig.